In the Claims:

1. (previously presented) A method of digital communication between two devices, said method comprising the steps of:

(1) a first device transmitting a predetermined bit pattern to a second device responsive to an instruction to transmit said predetermined bit pattern in a first time slot of a next frame and a start of said next frame signal transmitted from said second device using a clock signal transmitted from said second device;

(2) said second device sampling for bits of said predetermined bit pattern at sampling times determined by one of a rising edge or a falling edge of said clock signal beginning a delay period after said start of said next frame signal;

(3) if said second device does not detect said predetermined bit pattern, increasing said delay period by a fraction of a clock period and repeating steps (1) and (2), and, if necessary, step (3);

(4) if said second device detects said predetermined bit pattern, setting the last delay period used in step (2) as a delay period to be used by said second device for sampling data for further transmissions from said first device to said second device;

(5) said second device using said last delay period for sampling all further data transmissions from said first device to said second device; and,

wherein said second device performs step (2) twice before proceeding to steps (3) or (4).

2. (cancelled)

3. (previously presented) The method of claim 1 wherein said start of said next frame signal is a frame synchronization signal denoting a beginning of a frame.

4. (cancelled)

5. (previously presented) The method of claim 1 wherein said start of said next frame signal is transmitted on a first signal line, said predetermined bit pattern and all further

data is transmitted on a second signal line and a clock signal is transmitted on a third signal line and wherein transmissions on said second signal line and said sampling times are also a function of said clock signal.

6. (previously presented) The method of claim 5 wherein said digital communication is carried out under the control of a controller and is conducted between at least one target device.

7. (previously presented) The method of claim 6 wherein said clock signal is generated at said second device.

8. (previously presented) The method of claim 6 wherein said first device is one of said at least one target devices and said second device is said controller.

9. (cancelled).

10. (original) The method of claim 5 wherein, in step (3), said delay is increased by one-half of a clock cycle.

11. (cancelled).

12. (previously presented) A method of digital communication between two devices, said method comprising the steps of:

(1) a first device transmitting a predetermined bit pattern to a second device responsive to an instruction to transmit said predetermined bit pattern in a first time slot of a next frame and a start of said next frame signal transmitted from said second device using a clock signal transmitted from said second device;

(2) said second device sampling for bits of said predetermined bit pattern at sampling times determined by one of a rising edge or a falling edge of said clock signal beginning a delay period after said start of said next frame signal;

(3) if said second device does not detect said predetermined bit pattern, increasing said delay period by a frAction of a clock period and repeating steps (1) and (2), and, if necessary, step (3);

(4) if said second device detects said predetermined bit pattern, setting the last delay period used in step (2) as a delay period to be used by said second device for sampling data for further transmissions from said first device to said second device;

(5) said second device using said last delay period for sampling further data transmissions from said first device to said second device; and

(6) said first device predicting arrival of said start signal and commencing transmission of data in anticipation of receipt of said start of said next frame_signal.

13. (previously presented) A communication device for receiving digital data from another device, said communication device comprising:

a receive port for receiving data transmitted to said communication device from another device;

a processor adapted to:

(a) sample data received at said receive port for a predetermined bit pattern at sampling times determined by one of a rising edge or a falling edge of a clock signal beginning delay period after a start of a next frame signal, said start of a next frame signal transmitted by said communication device and initiating transmittal of said predetermined bit pattern by said other device using a clock signal transmitted from said second device;

(b) if said communication device detects said predetermined bit pattern, setting the delay period last used in step (a) as a delay period to be used by said communication device for sampling data; and

(c) if said communication device does not detect said predetermined bit pattern, increasing said delay period by a frAction of a clock period and repeating step (a) and step (b) or (c);

(d) using said last delay period for sampling further data transmissions; and

wherein said processor performs step (a) twice before proceeding to steps (b) or (c).

14. (previously presented) The communication device of claim 13 further comprising:

means for generating said start of a next frame signal; and

a second port for transmitting said start of a next frame signal to another device.

15. (previously presented) The communication device of claim 13 wherein said start of a next frame signal is a frame synchronization signal denoting a beginning of a frame.

16. (previously presented) The communication device of claim 14 further comprising means for generating [[a]] said clock signal; and

a third port for transmitting said clock signal to said other device and wherein transmission of said predetermined bit pattern and said sampling times also are a function of said clock signal.

17. (previously presented) The communication device of claim 16 wherein said digital communication is carried out under the control of a controller and is conducted between at least one target device.

18. (previously presented) The communication device of claim 17 wherein said communication device is said controller and said other device is said target device.

19. (currently amended) The communication device of claim 13 wherein said processor is further adapted to transmit an instruction to said other device, responsive to which said ~~other~~ another device transmits said predetermined bit pattern.

20. (previously presented) A method of receiving digital communication at a receiving device, said method comprising the steps of:

(1) receiving from a transmit device a predetermined bit pattern sent in response to a start of a next frame signal transmitted from said receiving device using a clock signal transmitted from said receiving device;

(2) sampling for bits of said predetermined bit pattern at sampling times determined by one of a rising edge or a falling edge of said clock signal beginning a delay period after said start of a next frame signal;

(3) if said predetermined bit pattern is not detected, increasing said delay period by a frAction of a clock period and repeating steps (1) and (2), and, if necessary, step (3);

(4) if said predetermined bit pattern is detected, setting a last said delay period used in step (2) as a delay period to be used for sampling data for further transmissions from said transmit device;

(5) using said last delay period for sampling further data communications from said transmit device; and,

wherein said second device performs step (2) twice before proceeding to steps (3) or (4).

21. (previously presented) A method of receiving digital communication at a receiving device, said method comprising the steps of:

(1) receiving from a transmit device a predetermined bit pattern sent in response to a start of a next frame signal transmitted from said receiving device, using a clock signal transmitted from said receiving device;

(2) sampling for bits of said predetermined bit pattern at sampling times determined by one of a rising edge or a falling edge of said clock signal beginning a delay period after said start of a next frame signal;

(3) if said predetermined bit pattern is not detected, increasing said delay period by a frAction of a clock period and repeating steps (1) and (2), and, if necessary, step (3);

(4) if said predetermined bit pattern is detected, setting a last said delay period used in step (2) as a delay period to be used for sampling data for further transmissions from said transmit device;

(5) using said last delay period for sampling further data communications from said transmit device; and

(6) said transmit device predicting arrival of said start of a next frame signal and commencing transmission of data in anticipation of receipt of said start of a next frame signal.

22. (cancelled)

23. (previously presented) The method of claim 12 wherein said start of said next frame signal is a frame synchronization signal denoting a beginning of a frame.

24. (canceled).

25. (previously presented) The method of claim 12 wherein said start of said next frame signal is transmitted on a first signal line, said predetermined bit pattern and all further data is transmitted on a second signal line and a clock signal is transmitted on a third signal line and wherein transmissions on said second signal line and said sampling times are also a function of said clock signal.

26. (previously presented) The method of claim 25 wherein said digital communication is carried out under the control of a controller and is conducted between at least one target device.

27. (previously presented) The method of claim 26 wherein said start of said next frame signal and said clock signal are generated at said second device.

28. (previously presented) The method of claim 26 wherein said first device is one of said at least one target devices and said second device is said controller.

29. (cancelled)

30. (previously presented) The method of claim 25 wherein, in step (3), said delay is increased by one-half of a clock cycle.

31. (previously presented) A communication system comprising a transmitting device and a communication device,

wherein said communication device comprises:

a receive port for receiving data transmitted to
said communication device from said transmitting device;
a receiver processor adapted to:
(a) sample data received at said receive port for a predetermined bit pattern at sampling times determined by one of a rising edge or falling edge of a clock signal beginning a delay period after a start of a next frame signal, said start of a next frame signal transmitted by said communication device and initiating transmittal of said predetermined bit pattern by said other device using said clock signal transmitted by said communication device ;
(b) if said communication device detects said predetermined bit pattern, setting the delay period last used in step (a) as a delay period to be used by said communication device for sampling data; and
(c) if said communication device does not detect said predetermined bit pattern, increasing said delay period by a frAction of a clock period and repeating step (a) and step (b) or (c); and
(d) using said last delay period for sampling further data transmissions;

and,

wherein said transmitting device comprises a transmitter processor adapted to predicting arrival of said start signal and commencing transmission of data in anticipation of receipt of said start of a next frame signal.

32. (previously presented) The communication device of claim 31 further comprising:

means for generating said start of a next frame signal; and

a second port for transmitting said start of a next frame signal to said transmitting device.

33. (cancelled).

34. (previously presented) The communication device of claim 32 further comprising means for generating [[a]] said clock signal; and

a third port for transmitting said clock signal to said transmitting device and wherein transmission of said predetermined bit pattern and said sampling times also are a function of said clock signal.

35. (currently amended) The communication device of claim 34 wherein said ~~digital communication~~ data is ~~carried out~~ transmitted under the control of a controller and is conducted between said communication device and at least one target device.

36. (currently amended) The communication device of claim 35 wherein said communication device is said controller and said ~~other~~ transmitting device is said target device.

37. (currently amended) The communication device of claim 31 wherein said receiver processor is further adapted to transmit an instruction to said ~~other~~ transmitting device, responsive to which said ~~other~~ transmitting device transmits said predetermined bit pattern.